Zone 3 Connector Pin Assignment Recommendation for RF Applications between AMC and RTM Boards in the MTCA.4 Standard

Features

MTCA.4 management zone:
- Power, I²C, optional JTAG support

Gigabit-Link zone:
- 1 Gigabit Transceiver Link
- 7 additional Gigabit Transmitter Links

User signal transmission zone:
- 6 LVDS inputs/outputs for user-configuration
- 3 LVDS outputs with fixed direction

Digital clock signal transmission zone:
- 5 LVDS/LVPECL differential inputs for low-jitter clock signals
- 2 LVDS/LVPECL output clock signals
- JESD204B Subclass 1 Compliant interface

Analog signal transmission zone:
- 8 channel AC/DC-coupled single-ended input signals (ADC)
- 4 channel AC/DC-coupled single-ended output signals (DAC)

Applications

- AMC / RTM board design in MTCA.4 standard
- Multi-channel analog-to-digital converters
- Multi-channel signal shaper
- Multi-channel sensor readout and output
- Analog signal conditioning boards
- Low-jitter clock signal sampling and clock recovery

General Description

This Class RF1.0 pin assignment definition of the Zone 3 connector in the MTCA.4 standard is a recommendation mainly for AMC and RTM boards transferring up to 12 analog signals over the Zone 3 connectors. This RF-class is designed for a three row ADF and two six pin coaxial connectors. The main goal is to classify the undefined Zone 3 pin assignment for applications to achieve a high compatibility between AMC and RTM boards.

This Class RF1.0 pin assignment requires a common RTM management implementation to make AMC and RTM boards compatible. Appropriate management interface templates for this Class are available on mtca.desy.de.

AMC ZONE 3 CONNECTOR PIN ASSIGNMENT RECOMMENDATION

		Digital Clock IO	Digital fixed IO	Digital Clock Input	Digital user IO		Standard Gbit-Links			MTCA.4 Management	
J30		10	9	8	7	6	5	4	3	2	1
-	f	AMC-CLK-	OUT1-/D7-	RF-CLK3-	D5-	D2-	GBT7-TX-	GBT4-TX-	GBT1-TX-	TMS	TDO
+	e	AMC-CLK+	OUT1+/D7+	RF-CLK3+	D5+	D2+	GBT7-TX+	GBT4-TX+	GBT1-TX+	TDI	TCK
-	d	RF-CLK2-	OUT0-/D6-	RF-CLK1-	D4-	D1-	GBT6-TX-	GBT3-TX-	GBT0-TX-	SCL	SDA
+	c	RF-CLK2+	OUT0+/D6+	RF-CLK1+	D4+	D1+	GBT6-TX+	GBT3-TX+	GBT0-TX+	MP	PS#
-	b	RF-CLK0-	AMC-TCLK-	RTM-CLK-	D3-	D0-CC-	GBT5-TX-	GBT2-TX-	GBT0-RX-	PWRB2	PWRB1
+	a	RF-CLK0+	AMC-TCLK+	RTM-CLK+	D3+	D0-CC+	GBT5-TX+	GBT2-TX+	GBT0-RX+	PWRA2	PWRA1

		Single Ended Analog Signals		
J31		3	2	1
	B	ADC-IN7	DAC-OUT1	DAC-OUT3
	A	ADC-IN6	DAC-OUT0	DAC-OUT2
J32		3	2	1
	B	ADC-IN1	ADC-IN3	ADC-IN5
	A	ADC-IN0	ADC-IN2	ADC-IN4

Table 1: Zone 3 - Class RF1.0 pin assignment J30, J31 and J32 connector, AMC side view

Notkestr. 85, 22607 Hamburg, GERMANY
M-Division, MSK - Group, www.desy.de
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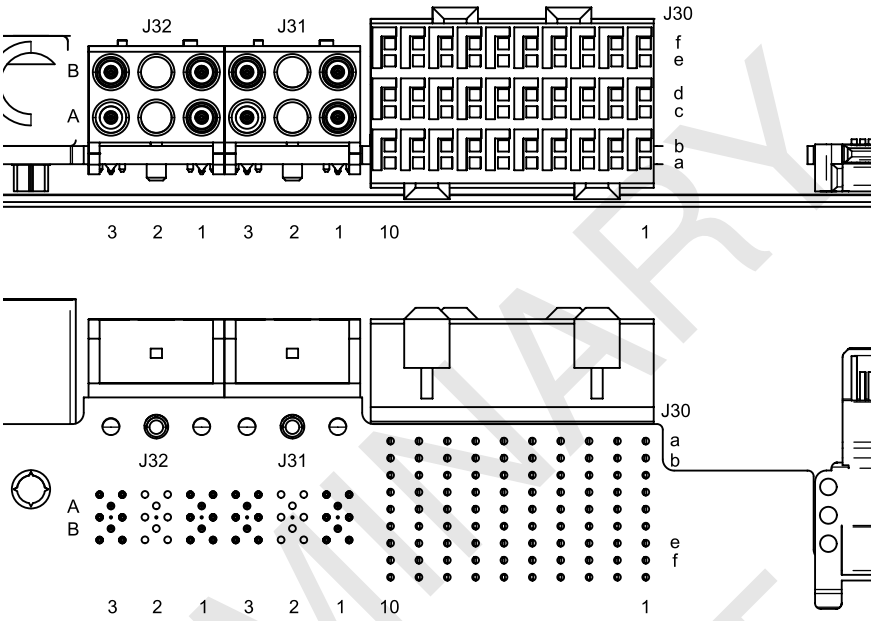

Figure 1: Zone 3 connectors AMC back side view (above), bottom view (below)

Zone 3 Class RF1.0 Pin Description

This Class RF1.0 is mainly used for high speed data acquisition applications having a maximum of twelve analog signal channels. As depicted in table 1, the zones in the analog Class RF1.0 consists of MTCA.4 Management, Standard Gigabit-Links, Digital IOs, clocks and a zone for single-ended analog signals. The management zone (J30 columns 1-2) is reserved for the RTM management in the MTCA.4 standard. The Standard Gbit-Links (J30 columns 3-5) houses the multi-gigabit transceivers. There is 1 bi-directional MGT (GBT0-RX/TX±) and 7 MGTs with fixed direction (GBT1..7-TX±) to establish a JESD204B interface with a DAC. Digital IO section consists of input/output signals in LVDS, CMOS or open collector (OC) level, which can be used for general purpose, e.g. I^2C communication for slow board diagnostics. To achieve a high compatibility between AMC and RTM boards, these inputs and outputs should be connected and programmable in direction and signal type, preferable by an FPGA located on the AMC side. If a high-speed parallel LVDS interface is needed in Digital User IO Zone, there is a clock capable differential pair (D0-CC±) that has to carry the interface clock. The Digital fixed IO zone (J30 column 8) houses LVDS output signals with fixed signal direction to provide a stable timing signal AMC-TCLK, which is the splitted TCLKA and two general purpose output signals OUT0 and OUT1 to the RTM, which can be used as differential user IOs. Digital Clock Input and IO zone (J30 column 8 and 10) offers 4 digital AC-coupled differential inputs (RF-CLK0..3±) to the AMC which should drive ADC clock inputs, 1 LVDS input (RTM-CLK±) and 1 LVDS output (AMC-CLK±) for low-jitter clock signals. RTM-CLK±and AMC-CLK±can be used to realize a JESD204B compliant interface on the RTM side.

The analog zone (J31 and J32) consists of up to 8 AC/DC-coupled single-ended analog input signals to the AMC (ADC-IN0..7) and 4 AC/DC-coupled single-ended analog outputs to the RTM (DAC-OUT0..3).

J30 connector			
PIN		I/O	DESCRIPTION
NAME	NUMBER		
PWRA1, PWRA2, PWRB1, PWRB2	1a, 2a, 1b, 2b	I	RTM supply voltage (12 V, 25 W max.)
PS#	1c	O	RTM present signal (connected to GND on RTM)
SDA, SCL	1d, 2d	I/O	I^2C management interface to RTM (level 3.3 V)
TCK, TDI, TDO, TMS	1e, 2e, 1f, 2f	I/O	JTAG interface to RTM
GBT0-RX0±	3a, 3b	I	gigabit transceiver (GBT) link 0 receiver pair (must be AC-coupled near receiver on AMC side)
GBT0-TX0±	3c, 3d	O	GBT link 0 transmitter pair (must be AC-coupled near receiver on RTM side)
GBT1-TX±, GBT2-TX±, GBT3-TX±, GBT4-TX±, GBT5-TX±, GBT6-TX±, GBT7-TX±	3e, 3f, 4a, 4b, 4c, 4d, 4e, 4f	O	GBT links 1 ... 7 transmitter pairs (must be AC-coupled near receiver on RTM side)
D0-CC±	6a, 6b	I/O	LVDS digital IO pair 0 clock capable
D1±, D2±, D3±, D4±, D5±	6c, 6d, 6e, 6f, 7a, 7b, 7c, 7d, 7e, 7f	I/O	LVDS digital IO pairs 1 ... 5
RTM-CLK±	8a, 8b	I	LVDS/LVPECL clock input from RTM
RF-CLK0±, ..., RF-CLK3	10a, 10b, 8c, 8d, 10c, 10d, 8e, 8f	I	LVDS/LVPECL clock inputs from RTM to drive ADC clock inputs
AMC-TCLK±	9a, 9b	O	LVDS/LVPECL clock output to RTM derived from telecommunication clock (JESD204B: SYSRef)
OUT0/D6±, OUT1/D7±	9c, 9d, 9e, 9f	I/O	LVDS output pairs 0, 1 (trigger, interlock) / LVDS digital IO pairs 6, 7
AMC-CLK±	10e, 10f	O	LVDS/LVPECL output clocks to RTM (JESD204B: Device Clock)

Table 2: Pin description J30 connector

J31 connector			
PIN		I/O	DESCRIPTION
NAME	NUMBER		
DAC-OUT0, DAC-OUT1, DAC-OUT2, DAC-OUT3	2A, 2B, 1A, 1B	O	RF DAC output signals (TODO: spec)
ADC-IN6, ADC-IN7	3A, 3B	I	RF ADC input signals (TODO: spec)

Table 3: Pin description J31 connector

J32 connector			
PIN		I/O	DESCRIPTION
NAME	NUMBER		
ADC-IN0, ADC-IN1, ADC-IN2, ADC-IN3, ADC-IN4, ADC-IN5	3A, 3B, 2A, 2B, 1A, 1B	I	RF ADC input signals (TODO: spec)

Table 4: Pin description J31 connector

Sequence of Signal Occupation

To achieve a high compatibility between AMC and RTM boards we recommend to use the sequence for the signal occupation in each zone starting from minimum label to the maximum in each zone. The signal distribution and filling sequence of

the clock and analog signals over Zone 3 is chosen for having a high isolation between these signals. Taken into account, that analog applications may need also a fast digital serial connection (J30 columns 3-5), the user zone starts at J30 column 6 and 7, where a user I2C bus for basic diagnostics can be placed. Digital output signals are located in (J30 column 9).

Analog inputs:	ADC-IN0, ADC-IN1, ..., ADC-IN7
Analog outputs	DAC-OUT0, ..., DAC-OUT3
Gigabit Transceiver Links:	(GBT0-RX±, GBT0-TX±), GBT1-TX±, ..., GBT7-TX±
Digital clock input signals:	RTM-CLK± *reserved for main ADC clock domain*
	RF-CLK0±, ..., RF-CLK3± *can be used to drive ADC clock inputs*
Digital clock output signals:	AMC-CLK±
Digital fixed output signals:	AMC-TCLK±, OUT0/D6±, OUT1/D7± *reserved for TCLK and trigger/interlock signals*
User - input/output signals:	D0-CC± *clock capable*, D1±, ..., D5± *user IO*, OUT0/D6±, OUT1/D7± *user IO, if no interlocks and trigger needed*

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