Zone 3 Connector Pin Assignment Recommendation for Analog Applications for AMC/µRTM Boards in the MTCA.4 standard

FEATURES

MTCA.4 management zone:
- Power, I²C, optional JTAG support

Analog signal transmission zone:
- 32 channel DC-coupled differential input signals
- 4 channel DC-coupled differential output signals

Digital clock signal transmission zone:
- 2 AC-coupled differential inputs for low-jitter clock signals
- 1 LVDS output clock signal

User signal transmission zone:
- 6 LVDS inputs / outputs for user-configuration
- 3 LVDS outputs with fixed output direction
- Optional dual high-speed link

Zone shielding:
- Supports ground shielding between zones

APPLICATIONS

- AMC / µRTM board design in MTCA.4 standard
- Multi-channel analog-to-digital converters
- Multi-channel signal shaper
- Multi-channel sensor readout and output
- Analog signal conditioning boards
- Low-jitter clock signal sampling and clock recovery

GENERAL DESCRIPTION

This Class A2.1 pin assignment definition of the Zone 3 connector in the MTCA.4 standard is a recommendation mainly for AMC and µRTM boards transferring a high number of analog signals over the Zone 3 connector. This analog class is designed for two three row ADF Zone 3 connectors and AMC modules having an FPGA. The main goal is to classify the undefined Zone 3 pin assignment for applications to achieve a high compatibility between AMC and µRTM boards.

This Class A2.1 pin assignment requires a common µRTM management implementation to make AMC and µRTM boards compatible. Appropriate management interface templates for this Class are available on http://mtca.desy.de.

AMC ZONE 3 CONNECTOR PIN ASSIGNMENT RECOMMENDATION

Class A2.1 / Zone			a	b	c	d	e	f
MTCA.4 management	J30	1	PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2	PWRA2	PWRB2	MP	SCL	TDI	TMS
Standard Gbit-Link		3	SFP-CLK+	SFP-CLK-	SFP-RX+	SFP-RX-	SFP-TX+	SFP-TX-
User-configuration		4	D3+	D3-	D4+	D4-	D5+	D5-
		5	D6+	D6-	D7+	D7-	D8+	D8-
Digital fixed I/O		6	AMC_TCLK+	AMC_TCLK-	OUT0+	OUT0-	OUT1+	OUT1-
Shielding		7	gnd	gnd	gnd	gnd	gnd	gnd
Digital clock inputs / Analog Signals		8	AMC_CLK0+	AMC_CLK0-	DAC3+	DAC3-	DAC2+	DAC2-
		9	RTM_CLK0+	RTM_CLK0-	DAC1+	DAC1-	DAC0+	DAC0-
		10	RTM_CLK1+	RTM_CLK1-	CH31+	CH31-	CH30+	CH30-
Analog signals	J31	1	CH29+	CH29-	CH28+	CH28-	CH27+	CH27-
		2	CH26+	CH26-	CH25+	CH25-	CH24+	CH24-
		3	CH23+	CH23-	CH22+	CH22-	CH21+	CH21-
		4	CH20+	CH20-	CH19+	CH19-	CH18+	CH18-
		5	CH17+	CH17-	CH16+	CH16-	CH15+	CH15-
		6	CH14+	CH14-	CH13+	CH13-	CH12+	CH12-
		7	CH11+	CH11-	CH10+	CH10-	CH9+	CH9-
		8	CH8+	CH8-	CH7+	CH7-	CH6+	CH6-
		9	CH5+	CH5-	CH4+	CH4-	CH3+	CH3-
		10	CH2+	CH2-	CH1+	CH1-	CH0+	CH0-

Table 1 : Pin assignment of Class A2.1, AMC side view

ZONE DESCRIPTION

This Class A2.1 is mainly used for data acquisition applications having a high number of analog signal channels. As depicted in Table 1, the zones in the analog Class A2.1 consists of a management zone, user zone, digital clock zone and a zone for analog differential signals..

The management zone (J30 row 1-2) is reserved for the µRTM management in the MTCA.4 standard. The user zone (J30 row 4-5) houses input and output signals in LVDS, CMOS or open collector (OC) level, which can be used for general purpose, e.g. I²C communication for slow board diagnostics. To achieve a high compatibility between AMC and µRTM boards, these inputs and outputs should be connected and programmable in direction and signal type, preferable by an FPGA located on the AMC side.

The user zone (J30 row 6) houses LVDS output signals with fixed signal direction to provide a stable timing signal AMC_TCLK, which is the splitted TCLKA and two general purpose output signals OUT0 and OUT1 to the µRTM typically not driving from the FPGA. The user zone (J30 row 3) offers one high speed link for general purposes. In case of not using the high speed link it is recommended to switch it off. The digital clock zone (J30 row 8-9) offers 2 digital AC-coupled differential inputs and 1 LVDS output AMC_CLK0 for low-jitter clock signals. RTM_CLK0 is reserved for the main ADC clock domain. The second clock RTM_CLK1 is optional and can be used for DACs or ADCs.

The analog zone (J31) consists of up to 32 analog DC-coupled differential signal inputs (CHx+, CHx-) and 4 DC-coupled differential outputs signals for current driven DACs (DACx+, DACx-).

SEQUENCE OF SIGNAL OCCUPATION

To achieve a high compatibility between AMC and µRTM boards we recommend to use the sequence for the signal occupation in each zone starting from minimum label to the maximum in each zone. The signal distribution and filling sequence of the clock and analog signals over Zone 3 is chosen for having a high isolation between these signals. Taken into account, that analog applications may need also a fast digital serial connection (J30 row 3), the user zone starts at J30 4ab, where a user I^2C bus for basic diagnostics can be placed. Digital output signals are located in (J30 row 6). (RTM_CLK1+, RTM_CLK1-) is reserved for a second clock domain for DACs or ADCs.

Analog inputs:	(CH0+, CH0-), (CH1+, CH1-),…, (CH31+, CH31-)
Analog outputs:	(DAC0+, DAC0-), (DAC1+, DAC1-), …, (DAC3+, DAC3-)
Digital input signals:	(RTM_CLK0+, RTM_CLK0-) reserved for main ADC clock domain
	(RTM_CLK1+, RTM_CLK1-) optionally reserved for DAC or ADC clocks
Digital output signals:	(AMC_CLK0+, AMC_CLK0-)
User - input/output signals:	(D3+,D3-), (D4+,D4-), … , (D8+, D8-)

AMC ZONE 3 CONNECTOR ELECTRICAL SPECIFICATION RECOMMENDATION

Class A2.1 / Zone			a	b	c	d	e	f
MTCA.4 management	J30	1	PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2	PWRA2	PWRB2	MP	SCL	TDI	TMS
Standard Gbit-Link		3	LVDS - I	LVDS - I	CML - I	CML - I	CML - O	CML - O
User-configuration		4	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
		5	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O	LVDS / LVCMOS / OC - I/O
Digital fixed I/O		6	LDVS - O	LDVS - O	LDVS - O	LDVS - O	LDVS - O	LDVS - O
Shielding		7	gnd	gnd	gnd	gnd	gnd	gnd
Digital clock inputs / Analog Signals		8	LDVS - O	LDVS - O	Differential 0 - ±20mA / 0 - ±1V / O, 100Ω		Differential 0 - ±20mA / 0 - ±1V / O, 100Ω	
		9	Differential AC-coupled, ±350mV…±1V / I, 100Ω		Differential 0 - ±20mA / 0 - ±1V / O, 100Ω		Differential 0 - ±20mA / 0 - ±1V / O, 100Ω	
		10	Differential AC-coupled, ±350mV…±1V / I, 100Ω		Differential 0 - ±1V / I, 100Ω		Differential 0 - ±1V / I, 100Ω	
Analog signals	J31	1	Differential 0 - ±1V / I, 100Ω		Differential 0 - ±1V / I, 100Ω		Differential 0 - ±1V / I, 100Ω	
		2	Differential 0 - ±1V / I, 100Ω		Differential 0 - ±1V / I, 100Ω		Differential 0 - ±1V / I, 100Ω	
		3	Differential 0 - ±1V / I, 100Ω		Differential 0 - ±1V / I, 100Ω		Differential 0 - ±1V / I, 100Ω	
		4	Differential 0 - ±1V / I, 100Ω		Differential 0 - ±1V / I, 100Ω		Differential 0 - ±1V / I, 100Ω	
		5	Differential 0 - ±1V / I, 100Ω		Differential 0 - ±1V / I, 100Ω		Differential 0 - ±1V / I, 100Ω	
		6	Differential 0 - ±1V / I, 100Ω		Differential 0 - ±1V / I, 100Ω		Differential 0 - ±1V / I, 100Ω	
		7	Differential 0 - ±1V / I, 100Ω		Differential 0 - ±1V / I, 100Ω		Differential 0 - ±1V / I, 100Ω	
		8	Differential 0 - ±1V / I, 100Ω		Differential 0 - ±1V / I, 100Ω		Differential 0 - ±1V / I, 100Ω	
		9	Differential 0 - ±1V / I, 100Ω		Differential 0 - ±1V / I, 100Ω		Differential 0 - ±1V / I, 100Ω	
		10	Differential 0 - ±1V / I, 100Ω		Differential 0 - ±1V / I, 100Ω		Differential 0 - ±1V / I, 100Ω	

Table 2: Electrical specification of Class A2.1 (“I”=input (µRTM to AMC), “O”=output (AMC to µRTM)), AMC side view

The signals of the management zone are defined in PICMG MTCA.4 R1.0, Section 4. The high speed link signals (J30 row 3) have fixed signal direction, level of LVDS for an external clock and CML for receiving and transmitting data. Digital levels in the user zone (J30 row 3-4) are LVDS, LVCMOS or open collector (OC) outputs typically provided by an FPGA. LVCMOS or OC outputs needs on the µRTM a supply voltage adjust mechanism controlled by the AMC management. Using I^2C communication open collector signals in the user zone are assumed to be terminated on the µRTM side. Digital output signals (J30 row 6) and signals of the clock and analog zone (J30 row 8,9,10) have fixed direction. Digital low-jitter clock input signals (J30 9ab, 10ab) are AC-coupled differential signals in the range of 350mV… 1V. This allows the usage of LVDS, LVPECL, CML and other digital low-jitter signal types. The AC-coupling is done before termination on the AMC-side. Signals of the analog zone (J31) are typically in the range of -1V…+1V and have to be differentially matched by 100 Ohms defined by the ADF connector. For optimal performance the analog outputs should be current driven typically in the range of -20mA…+20mA.

AMC MODULE AND µRTM PROTECTION

According to the PICMG MTCA.4 R1.0, section 3.5.7, ¶79 the insertion and extraction process of an µRTM need an application specific quiesce action, e.g. no action, isolation of signals or powering off the AMC controlled by the MMC. All AMC output signals with fixed direction of Class A2.1 compatible modules have to be disabled via buffers on the AMC side controlled by the MMC. In addition these signals can be disabled or enabled application specific independent of the MMC protection mechanism.

Modern FPGAs offer a wide range of single- and differential ended input and output levels using different supply voltage banks. Here LVDS, LVCMOS_25, CML and open collector signaling with 2.5V power supply in the user zone are of interest. FPGA signals can be isolated during the insertion process, other devices rather not. Most of the devices have inputs and outputs protected with diodes intended only for short transient currents, as depicted in Fig.1. In case of an unpowered µRTM, active high state output stages of the AMC module will continuously dissipate power into the µRTM protection diodes. Depending on the output stages of Fig.2 the maximum short-to-GND currents are given by 40mA for LVDS, 50mA for CML, 200mA for LVCMOS_25 and approx. 2.5mA for OC_25 (open collector). AMC and µRTM boards for analog applications, that uses analog voltages in the range of -1V…1V must have a N=2 module hardware keying according to the MTCA.4 standard listed in Table 3, respectively N=3 when using LVCMOS_25 in the user zone.

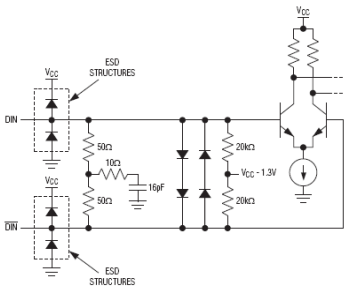


Fig.1 : Differential input stage

N	Data Signal in Volts
1	LVDS
2	0 – ±1
3	>±1 – ±3.3
4	>±3.3 – ±10
5	>±10
6	Reserved
7	Reserved
8	Reserved

Table 3: Mechanical module keying

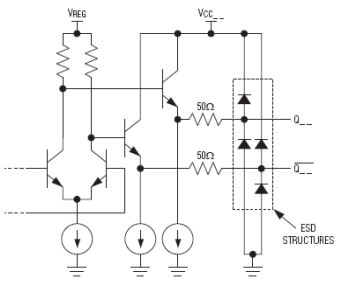
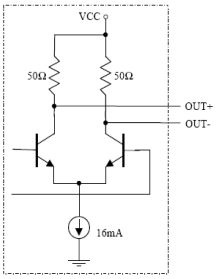
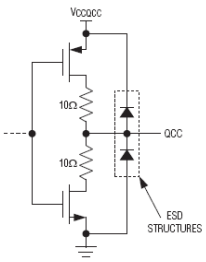


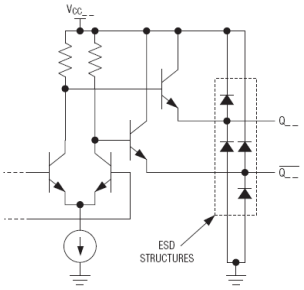
Fig.2: (a) LVDS output stage



(b) CML output stage



(c) LVCMOS output stage



(d) LVPECL output stage

Table 4 shows the AMC output signals, which have to be isolated, disabled or tri-stated on the AMC side in Class A2.1. Depending on the signal type the recommended protection method is listed. The FPGA gets the disabling information directly from MMC.

Idle state, AC-coupled	(SFP-TX+, SFP-TX-) state should be set to IDLE mode by FPGA on the AMC and µRTM. To remove common mode CML-levels, an AC-coupling has to be used on each transceiver side.
Disabling via FPGA	FPGA signals of the user zone (J30 row 4,5) can be disabled via FPGA itself.
Disabling via buffer	LDVS output signals (J30 row 4,5) with fixed signal direction have to be disabled by using a buffer with output enable. The disabling information is provided by the MMC. Depending on the application the buffer speed and jitter performance has to be chosen.
DAC quiescent condition	The DAC quiescent condition for a current driven DAC is a zero output current or power down. To reduce transient voltages for an unmatched current driven DAC output in case of an unplugged µRTM, a matching network on the AMC and µRTM is recommended. Isolating DAC outputs via analog buffers will degrade the performance and is not an option.

Class A2.1 / Zone			a	b	c	d	e	f
MTCA.4 management	J30	1						
		2						
Standard Gbit-Link		3			Idle state, RTM AC-coupled	Idle state, RTM AC-coupled	Idle state, AMC AC-coupled	Idle state, AMC AC-coupled
User-configuration		4	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		5	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
Digital fixed I/O		6	Disabling via Buffer	Disabling via Buffer	Disabling via Buffer	Disabling via Buffer	Disabling via Buffer	Disabling via Buffer
Shielding		7						
Digital clock inputs / Analog Signals		8	Disabling via Buffer	Disabling via Buffer	DAC quiescent condition	DAC quiescent condition	DAC quiescent condition	DAC quiescent condition
		9			DAC quiescent condition	DAC quiescent condition	DAC quiescent condition	DAC quiescent condition
		10						
Analog signals	J31	1						
		2						
		3						
		4						
		5						
		6						
		7						
		8						
		9						
		10						

Table 4: Quiescent signal conditions of Class A2.1, AMC side view

After inserting the µRTM a compatibility check of the Zone 3 has to performed according to the MTCA.4. After successful acceptance, the µRTM payload power can be switched on. If an µRTM is extracted via hot-swap handle, the µRTM has to be switched off via MMC and the AMC has to set the Zone 3 signals into the disabled state, as well after power cuts and failures. All µRTM output signals do not have to be isolated, because they are powered down during the insertion process. Isolating analog or low-jitter clock signals will degrade their performance and is no option in this class.

ZONE 3 GROUNDING, SHIELDING AND TERMINATION

Each additional pin, which can be grounded on the AMC or µRTM side will increase the signal isolation for a given Zone 3 connector. Grounding both sides will improve the robustness of the AMC and µRTM against EMI distortions crossing the Zone 3. Unused input signals should be in general terminated on the receiver side. They must provide a defined default electrical state defined by the receiver side to avoid oscillations of the following circuit sections. The following guideline should be used if the AMC or the µRTM does not support a signal function.

Standard Gbit Link: If the µRTM do not support SFP, the SFP-CLK and SFP-Rx signal of the AMC should be open on the µRTM side.
If the µRTM do not support SFP, the SFP-Tx signal of the AMC should be terminated on the µRTM side.
If the AMC do not support SFP, the AMC should terminate SFP-CLK and SFP-Rx.
If the AMC do not support SFP, the AMC signal SFP-Tx should be open.

User configuration: The µRTM should let all unused signals open.
The AMC should let all unused signals open.

Digital fixed I/O: If the µRTM do not support the signal function, the µRTM should terminate signals of this group.
If AMC_TCLK, OUT0 or OUT1 is not used (implemented) by the AMC, it should let them open.
If the µRTM support the signal function it has to provide a default logic state for the signals OUT0 and OUT1.

Digital clock inputs: Unused digital clock inputs should be grounded on the µRTM side, signals are AC-coupled on the AMC side.
Unused digital clock inputs should be terminated on the AMC side.

Analog inputs: Unused analog AC-input or DC-input ports should be grounded on the µRTM.
Unused analog AC-input or DC-input ports should be shorted on the µRTM rear signal inputs to avoid oscillations at Zone 3.
Unused analog AC-input or DC-input ports can be open, terminated or grounded on the AMC side:

Open	: Recommended, especially if space and routing for a termination degrade the performance.
Terminated	: Can be used if space and routing for a termination do not degrade the performance.
(*) Grounded	: The AMC may only ground them if a functional or electrical compatibility check of Zone 3 is used. The robustness of boards against EMI is improved, but only compatible boards will be activated.

Analog outputs: Unused current driven DACs should be grounded on the µRTM.
Unused analog outputs should be grounded on the AMC.

Table 5 and Table 6 shows the signal termination if the AMC, respectively µRTM does not support a signal function. In case of not using the high speed link it should be switched off to avoid crosstalk onto the µRTM. Unused AC-input or DC-input ports should be open. Their rear signal inputs on the µRTM should be shorted to avoid oscillations at Zone 3. IF unused AC-input or DC-input ports are grounded to improve the EMI robustness only compatible boards will be activated via E-keying.

Class A2.1 / Zone			**a**	**b**	**c**	**d**	**e**	**f**
AMC side								
MTCA.4 management	J30	**1**	PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2	PWRA2	PWRB2	MP	SCL	TDI	TMS
Standard Gbit-Link		**3**	differential terminated		differential terminated		open	open
User-configuration		**4**	open	open	open	open	open	open
		5	open	open	open	open	open	open
Digital fixed I/O		**6**	open	open	open	open	open	open
Shielding		**7**	gnd	gnd	gnd	gnd	gnd	gnd
Digital clock inputs / Analog Signals		**8**	open	open	gnd	gnd	gnd	gnd
		9	differential terminated		gnd	gnd	gnd	gnd
		10	differential terminated		open / differential terminated / gnd *		open / differential terminated / gnd *	
Analog signals	J31	**1**	open / differential terminated / gnd *		open / differential terminated / gnd *		open / differential terminated / gnd *	
		2	open / differential terminated / gnd *		open / differential terminated / gnd *		open / differential terminated / gnd *	
		3	open / differential terminated / gnd *		open / differential terminated / gnd *		open / differential terminated / gnd *	
		4	open / differential terminated / gnd *		open / differential terminated / gnd *		open / differential terminated / gnd *	
		5	open / differential terminated / gnd *		open / differential terminated / gnd *		open / differential terminated / gnd *	
		6	open / differential terminated / gnd *		open / differential terminated / gnd *		open / differential terminated / gnd *	
		7	open / differential terminated / gnd *		open / differential terminated / gnd *		open / differential terminated / gnd *	
		8	open / differential terminated / gnd *		open / differential terminated / gnd *		open / differential terminated / gnd *	
		9	open / differential terminated / gnd *		open / differential terminated / gnd *		open / differential terminated / gnd *	
		10	open / differential terminated / gnd *		open / differential terminated / gnd *		open / differential terminated / gnd *	

Table 5: Signal termination in Class A2.1 if the AMC does not support a signal function, AMC side view

Class A2.1 / Zone			**a**	**b**	**c**	**d**	**e**	**f**
RTM side								
MTCA.4 management	J30	**1**	PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2	PWRA2	PWRB2	MP	SCL	TDI	TMS
Standard Gbit-Link		**3**	open	open	open	open	differential terminated	
User-configuration		**4**	open	open	open	open	open	open
		5	open	open	open	open	open	open
Digital fixed I/O		**6**	differential terminated		differential terminated		differential terminated	
Shielding		**7**	gnd	gnd	gnd	gnd	gnd	gnd
Digital clock inputs / Analog Signals		**8**	differential terminated		gnd	gnd	gnd	gnd
		9	gnd	gnd	gnd	gnd	gnd	gnd
		10	gnd	gnd	gnd	gnd	gnd	gnd
Analog signals	J31	**1**	gnd	gnd	gnd	gnd	gnd	gnd
		2	gnd	gnd	gnd	gnd	gnd	gnd
		3	gnd	gnd	gnd	gnd	gnd	gnd
		4	gnd	gnd	gnd	gnd	gnd	gnd
		5	gnd	gnd	gnd	gnd	gnd	gnd
		6	gnd	gnd	gnd	gnd	gnd	gnd
		7	gnd	gnd	gnd	gnd	gnd	gnd
		8	gnd	gnd	gnd	gnd	gnd	gnd
		9	gnd	gnd	gnd	gnd	gnd	gnd
		10	gnd	gnd	gnd	gnd	gnd	gnd

Table 6: Signal termination in Class A2.1 if the µRTM does not support a signal function, µRTM side view

COMPATIBILITY TO ANALOG CLASS A1.1

Class A2.1 boards are not compatible to other classes. For test purpose with limited functionality, AMC and µRTM boards can be used between Class A1.1 and Class A.2.1. In this case the signals RTM_CLK1, CH30, CH31, CH1, CH7, CH13, CH19, CH25 should be unused or isolated on the µRTM side. RTM_CLK1, RTM_CLK2, RTM_CLK3, RTM_CLK5 on Class A1.1 compatible µRTM should be unused or isolated.

REVISION CHANGES AND HISTORY

2014/03	: - Introduce a new analog Class for a high number of up to 32 analog signals over Zone 3. For simplification Class A2.1 compatible boards are not compatible to Class A1.1. Making Class A2.1 compatible to Class A1.1 is only possible for a small number of channels.
2014/03 (Rev.A.1)	: - To simplify the Class usage the filling order of CHx signals in J31 is simplified compared to Class A1.1. A minor signal crosstalk degradation by approx. 10dB was accepted by TEWS.
2014/01 (Rev.A.1)	: - For time domain gating applications on the µRTM the AMC_CLK0 signal from AMC to µRTM is available.
2014/01 (Rev.A.1)	: - BoF group1 Zone 3 pin assignment (Class recommendation) Rev.A.1. to be confirmed.