Zone 3 Connector Pin Assignment Recommendation for Analog Applications for AMC/µRTM Boards in the MTCA.4 standard

FEATURES

MTCA.4 management zone:
- Power, I²C, optional JTag support

Analog signal transmission zone:
- 10 channel AC-coupled differential input signals
- 10 channel DC-coupled differential input signals
- 5 channel DC-coupled differential output signals

Digital clock signal transmission zone:
- 6 AC-coupled differential inputs for low-jitter clock signals

User signal transmission zone:
- 6-12 LVDS inputs / outputs for user-configuration
- Optional 3 LVDS outputs with fixed output direction
- Optional high-speed link

Zone shielding:
- Supports ground shielding between zones

APPLICATIONS

- AMC / µRTM board design in MTCA.4 standard
- High-precision multi-channel analog-to-digital converters
- High-speed multi-channel analog-to-digital converters
- Multi-channel high-frequency down/up-converters
- Multi-channel sensor readout and output
- Analog signal conditioning boards
- Low-jitter clock signal sampling and clock recovery

GENERAL DESCRIPTION

This Class A1 pin assignment definition of the Zone 3 connector in the MTCA.4 standard is a recommendation mainly for AMC and µRTM boards transferring analog signals over the Zone 3 connector. This analog class is designed for two three row ADF Zone 3 connectors and AMC modules having an FPGA. The main goal is to classify the undefined Zone 3 pin assignment for applications to achieve a high compatibility between AMC and µRTM boards.

This Class A1 pin assignment requires a common µRTM management implementation to make AMC and µRTM boards compatible. Appropriate management interface templates for this Class are available on http://mtca.desy.de.

AMC ZONE 3 CONNECTOR PIN ASSIGNMENT RECOMMENDATION

Class A1 / Zone			a	b	c	d	e	f
MTCA.4 management	J30	1	PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2	PWRA2	PWRB2	MP	SCL	TDI	TMS
FPGA / Standard Gbit-Link		3	D0+ / SFP-CLK+	D0- / SFP-CLK-	D1+ / SFP-RX+	D1- /SFP-RX-	D2+ / SFP-TX+	D2- / SFP-TX-
FPGA User-configuration		4	D3+	D3-	D4+	D4-	D5+	D5-
		5	D6+	D6-	D7+	D7-	D8+	D8-
FPGA / Digital fixed I/O		6	D9+ / AMC_TCLK+	D9- / AMC_TCLK-	D10+ / OUT0+	D10- / OUT0-	D11+ / OUT1+	D11- / OUT1-
Shielding		7	gnd	gnd	gnd	gnd	gnd	gnd
Digital clock inputs		8	RTM_CLK4+	RTM_CLK4-	RTM_CLK2+	RTM_CLK2-	RTM_CLK5+	RTM_CLK5+
		9	RTM_CLK0+	RTM_CLK0-	RTM_CLK3+	RTM_CLK3-	RTM_CLK1+	RTM_CLK1-
Shielding		10	gnd	gnd	gnd	gnd	gnd	gnd
Analog signals	J31	1	CH9_PA+	CH9_PA-	DAC0+	DAC0-	CH9_TF+	CH9_TF-
		2	CH8_TF+	CH8_TF-	gnd	gnd	CH8_PA+	CH8_PA-
		3	CH7_PA+	CH7_PA-	DAC1+	DAC1-	CH7_TF+	CH7_TF-
		4	CH6_TF+	CH6_TF-	gnd	gnd	CH6_PA+	CH6_PA-
		5	CH5_PA+	CH5_PA-	DAC2+	DAC2-	CH5_TF+	CH5_TF-
		6	CH4_TF+	CH4_TF-	gnd	gnd	CH4_PA+	CH4_PA-
		7	CH3_PA+	CH3_PA-	DAC3+	DAC3-	CH3_TF+	CH3_TF-
		8	CH2_TF+	CH2_TF-	gnd	gnd	CH2_PA+	CH2_PA-
		9	CH1_PA+	CH1_PA-	DAC4+	DAC4-	CH1_TF+	CH1_TF-
		10	CH0_TF+	CH0_TF-	gnd	gnd	CH0_PA+	CH0_PA-

Table 1 : Pin assignment of Class A1, AMC side view

ZONE DESCRIPTION

As depicted in Table 1, the zones in the analog Class A1 consists of a management zone, user zone, digital clock zone and a zone for analog differential signals. The signal placement and filling sequence is done such, that the most sensitive signals have to be filled-up from connector (J31 row 10) to (J30 row 3) and signals emitting high distortions filled-up vice versa.

The management zone (J30 row 1-2) is reserved for the µRTM management in the MTCA.4 standard. The user zone (J30 row 3-6) houses input and output signals in LVDS, CMOS or open collector (OC) level, which can be used for general purpose, e.g. I²C communication for slow board diagnostics. To achieve a high compatibility between AMC and µRTM boards, these inputs and outputs should be programmable in direction and signal type, preferable by an FPGA located on the AMC side.

Organized in different subclasses, described more in detail in the section subclass and class compatibility, the user zone (J30 row 6) can houses optionally LVDS output signals with fixed signal direction to provide a stable timing signal AMC_TCLK, which is the splitted TCLKA signal and two general purpose output signals OUT0 and OUT1 to the µRTM. The user zone (J30 row 3) offers optionally one high speed link for general purposes. In case of not using the high speed link or AMC_TCLK clock it is recommended to switch them off. The digital clock zone (J30 row 8-9) offers 6 digital AC-coupled differential inputs for low-jitter clock signals. RTM_CLK4 can be used for DAC clocks and RTM_CLK5 to synchronize FPGAs on the AMC side.

The analog zone (J31) consists of 10 analog AC-coupled differential signal inputs (CHx_TF+, CHx_TF-), 10 analog DC-coupled differential signal inputs (CHx_PA+, CHx_PA-) and 5 DC-coupled differential outputs signals for current driven DACs (DACx+, DACx-). The separation between AC- and DC-coupled inputs is caused by the fact, that low-noise applications usually require sophisticated AC-coupled transformer stages and broadband applications require DC-coupled operational amplifier input stages. See the more detailed description in the revision history.

SEQUENCE OF SIGNAL OCCUPATION

To achieve a high compatibility between AMC and µRTM boards we recommend to use the sequence for the signal occupation in each zone starting from minimum label to the maximum in each zone. The signal distribution and filling sequence of the clock and analog signals over Zone 3 is chosen for having the highest isolation between these signals. Taken into account, that analog applications may need also a fast digital serial connection (J30 row 3), the user zone starts at J30 4ab, where a user I²C bus for basic diagnostics can be placed. Digital output signals are located in (J30 row 6). (RTM_CLK4+, RTM_CLK4-) is reserved for DAC clocks and (RTM_CLK5+, RTM_CLK5-) for FPGA clocks located on the AMC side.

Analog DC-coupled inputs:	(CH0_PA+, CH0_PA-), (CH0_PA+, CH0_PA-),…, (CH9_PA+, CH9_PA-)
Analog AC-coupled inputs:	(CH0_TF+, CH0_TF-), (CH1_TF+,CH1_TF-),…, (CH9_TF+, CH9_TF-)
Analog outputs:	(DAC0+, DAC0-), (DAC1+, DAC1-), …, (DAC4+, DAC4-)
Digital input signals:	(RTM_CLK0+, RTM_CLK0-), (RTM_CLK1+, RTM_CLK1-),…, (RTM_CLK5+, RTM_CLK5-)
	(RTM_CLK4+, RTM_CLK4-) reserved for DAC clocks
	(RTM_CLK5+, RTM_CLK5-) reserved for FPGA clocks
User - input/output signals:	(D3+,D3-), (D4+,D4-), … , (D8+, D8-) ,
	optionally (D0+,D0-), (D1+,D1-), (D2+,D2-), (D9+,D9-), (D10+,D10-),, (D11+,D11-),
	optionally (OUT0+, OUT0-), (OUT1+, OUT1-)

AMC ZONE 3 CONNECTOR ELECTRICAL SPECIFICATION RECOMMENDATION

Class A1 / Zone			a	b	c	d	e	f
MTCA.4 management	J30	1	PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2	PWRA2	PWRB2	MP	SCL	TDI	TMS
FPGA / Standard Gbit-Link		3	LVDS/LVCMOS/OC-I/O or LVDS-I	LVDS/LVCMOS/OC-I/O or LVDS-I	LVDS/LVCMOS/OC-I/O or CML-I	LVDS/LVCMOS/OC-I/O or CML-I	LVDS/LVCMOS/OC-I/O or CML-O	LVDS/LVCMOS/OC-I/O or CML-O
FPGA User-configuration		4	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O
		5	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O
FPGA / Digital fixed I/O		6	LVDS/LVCMOS/OC-I/O or LDVS-O	LVDS/LVCMOS/OC-I/O or LDVS-O	LVDS/LVCMOS/OC-I/O or LDVS-O	LVDS/LVCMOS/OC-I/O or LDVS-O	LVDS/LVCMOS/OC-I/O or LDVS-O	LVDS/LVCMOS/OC-I/O or LDVS-O
Shielding		7	gnd	gnd	gnd	gnd	gnd	gnd
Digital clock inputs		8	Differential AC-coupled, ±350mV…±1V / I, 100Ω		Differential AC-coupled, ±350mV…±1V / I, 100Ω		Differential AC-coupled, ±350mV…±1V / I, 100Ω	
		9	Differential AC-coupled, ±350mV…±1V / I, 100Ω		Differential AC-coupled, ±350mV…±1V / I, 100Ω		Differential AC-coupled, ±350mV…±1V / I, 100Ω	
Shielding		10	gnd	gnd	gnd	gnd	gnd	gnd
Analog signals	J31	1	Differential 0 - ±1V / I, 100Ω		Differential 0 - ±20mA / 0 - ±1V / O, 100Ω		Differential 0 - ±1V / I, 100Ω	
		2	Differential 0 - ±1V / I, 100Ω		gnd	gnd	Differential 0 - ±1V / I, 100Ω	
		3	Differential 0 - ±1V / I, 100Ω		Differential 0 - ±20mA / 0 - ±1V / O, 100Ω		Differential 0 - ±1V / I, 100Ω	
		4	Differential 0 - ±1V / I, 100Ω		gnd	gnd	Differential 0 - ±1V / I, 100Ω	
		5	Differential 0 - ±1V / I, 100Ω		Differential 0 - ±20mA / 0 - ±1V / O, 100Ω		Differential 0 - ±1V / I, 100Ω	
		6	Differential 0 - ±1V / I, 100Ω		gnd	gnd	Differential 0 - ±1V / I, 100Ω	
		7	Differential 0 - ±1V / I, 100Ω		Differential 0 - ±20mA / 0 - ±1V / O, 100Ω		Differential 0 - ±1V / I, 100Ω	
		8	Differential 0 - ±1V / I, 100Ω		gnd	gnd	Differential 0 - ±1V / I, 100Ω	
		9	Differential 0 - ±1V / I, 100Ω		Differential 0 - ±20mA / 0 - ±1V / O, 100Ω		Differential 0 - ±1V / I, 100Ω	
		10	Differential 0 - ±1V / I, 100Ω		gnd	gnd	Differential 0 - ±1V / I, 100Ω	

Table 2: Electrical specification of Class A1 (“I”=input (µRTM to AMC), “O”=output (AMC to µRTM)), AMC side view

The signals of the management zone are defined in PICMG MTCA.4 R1.0, Section 4. The high speed link signals (J30 row 3) have fixed signal direction, level of LVDS for an external clock and CML for receiving and transmitting data. Digital levels in the user zone (J30 row 3-4) are LVDS, LVCMOS or open collector (OC) outputs typically provided by an FPGA. LVCMOS or OC outputs needs on the µRTM a supply voltage adjust mechanism controlled by the AMC management. Using I²C communication open collector signals in the user zone are assumed to be terminated on the µRTM side. Digital output signals (J30 row 6) and signals of the clock zone (J30 row 8,9) have fixed direction. Digital low-jitter clock input signals (J30 row 8,9) are AC-coupled differential signals in the range of ±350mV…±1V. This allows the usage of LVDS, LVPECL, CML and other digital low-jitter signal types. The AC-coupling is done before termination on the AMC-side. Signals of the analog zone (J31) are typically in the range of -1V…+1V and have to be differentially matched by 100 Ohms defined by the ADF connector. For optimal performance the analog outputs should be current driven typically in the range of -20mA…+20mA.

AMC MODULE AND µRTM PROTECTION

According to the PICMG MTCA.4 R1.0, section 3.5.7, ¶79 the insertion and extraction process of an µRTM need an application specific quiesce action, e.g. no action, isolation of signals or powering off the AMC controlled by the MMC. All AMC output signals with fixed direction of Class A1.1 compatible modules have to be disabled via buffers on the AMC side controlled by the MMC. In addition these signals can be disabled or enabled application specific independent of the MMC protection mechanism.

Modern FPGAs offer a wide range of single- and differential ended input and output levels using different supply voltage banks. Here LVDS, LVCMOS_25, CML and open collector signaling with 2.5V power supply in the user zone are of interest. FPGA signals can be isolated during the insertion process, other devices rather not. Most of the devices have inputs and outputs protected with diodes intended only for short transient currents, as depicted in Fig.1. In case of an unpowered µRTM, active high state output stages of the AMC module will continuously dissipate power into the µRTM protection diodes. Depending on the output stages of Fig.2 the maximum short-to-GND currents are given by 40mA for LVDS, 50mA for CML, 200mA for LVCMOS_25 and approx. 2.5mA for OC_25 (open collector). AMC and µRTM boards for analog applications, that uses analog voltages in the range of -1V…1V must have a N=2 module hardware keying according to the MTCA.4 standard listed in Table 3, respectively N=3 when using LVCMOS_25 in the user zone.

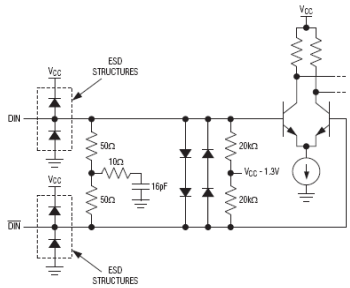


Fig.1 : Differential input stage

N	Data Signal in Volts
1	LVDS
2	0 – ±1
3	>±1 – ±3.3
4	>±3.3 – ±10
5	>±10
6	Reserved
7	Reserved
8	Reserved

Table 3: Mechanical module keying

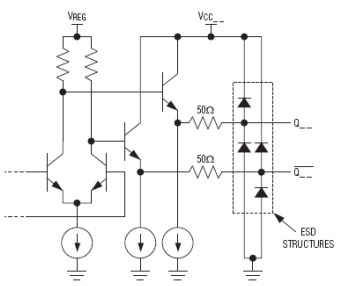
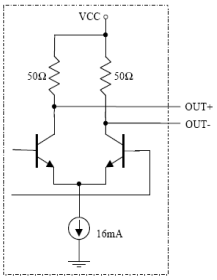
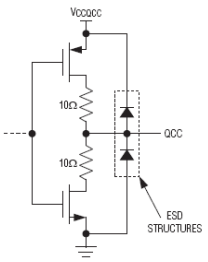


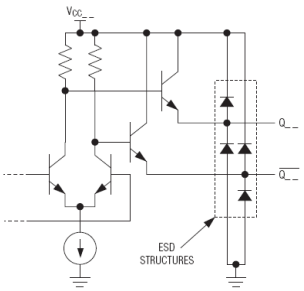
Fig.2: (a) LVDS output stage



(b) CML output stage



(c) LVCMOS output stage



(d) LVPECL output stage

Table 4 shows the AMC output signals, which have to be isolated, disabled or tri-stated on the AMC side in Class A1. Depending on the signal type the recommended protection method is listed. The FPGA gets the disabling information directly from MMC.

Idle state, AC-coupled	(SFP-TX+, SFP-TX-) state should be set to IDLE mode by FPGA on the AMC and µRTM. To remove common mode CML-levels, an AC-coupling must be done on the transmitter side. Optionally the receiver side can be AC-coupled using appropriate capacitors or 0Ohm jumpers.
Disabling via FPGA	FPGA signals of the user zone (J30 row 4,5) can be disabled via FPGA itself.
Disabling via buffer	LDVS output signals (J30 row 4,5) with fixed signal direction have to be disabled by using a buffer with output enable. The disabling information is provided by the MMC. Depending on the application the buffer speed and jitter performance has to be selected. For the AMC_TCLK signal a jitter of less than about 0.5ps is recommended.
DAC quiescent condition	The DAC quiescent condition for a current driven DAC is a zero output current or power down. To reduce transient voltages for an unmatched current driven DAC output in case of an unplugged µRTM, a matching network on the AMC and µRTM is recommended. Isolating DAC outputs via analog buffers will degrade the performance and is not an option.

Class A1 / Zone			a	b	c	d	e	f
MTCA.4 management	J30	1						
		2						
FPGA / Standard Gbit-Link		3	Disabling via FPGA / nothing	Disabling via FPGA / nothing	Disabling via FPGA / Idle state. RTM AC-coupled	Disabling via FPGA / Idle state. RTM AC-coupled	Disabling via FPGA / Idle state. AMC AC-coupled	Disabling via FPGA / Idle state. AMC AC-coupled
FPGA User-configuration		4	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		5	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
FPGA / Digital fixed I/O		6	Disabling via FPGA / Buffer	Disabling via FPGA / Buffer	Disabling via FPGA / Buffer	Disabling via FPGA / Buffer	Disabling via FPGA / Buffer	Disabling via FPGA / Buffer
Shielding		7						
Digital clock inputs		8						
		9						
Shielding		10						
Analog signals	J31	1			DAC quiescent condition	DAC quiescent condition		
		2						
		3			DAC quiescent condition	DAC quiescent condition		
		4						
		5			DAC quiescent condition	DAC quiescent condition		
		6						
		7			DAC quiescent condition	DAC quiescent condition		
		8						
		9			DAC quiescent condition	DAC quiescent condition		
		10						

Table 4: Quiescent signal conditions of Class A1, AMC side view

After inserting the µRTM a compatibility check of the Zone 3 has to performed according to the MTCA.4. After successful acceptance, the µRTM payload power can be switched on. If an µRTM is extracted via hot-swap handle, the µRTM has to be switched off via MMC and the AMC has to set the Zone 3 signals into the disabled state. After power cuts and failures the default Zone 3 state should be disabled. All µRTM output signals do not have to be isolated, because they are powered down during the insertion process. Isolating analog or low-jitter clock signals will degrade their performance and is no option in this class.

ZONE 3 GROUNDING, SHIELDING AND TERMINATION

Each additional pin, which can be grounded on the AMC or µRTM side will increase the signal isolation for a given Zone 3 connector. Grounding both sides will improve the robustness of the AMC and µRTM against EMI distortions crossing the Zone 3. Unused input signals should be in general terminated on the receiver side. They must provide a defined default electrical state defined by the receiver side to avoid oscillations of the following circuit sections. The following guideline should be used if the AMC or the µRTM do not support a signal function.

Standard Gbit Link:
If the µRTM do not support SFP, the SFP-CLK and SFP-Rx signal from AMC should be open on the µRTM side.
If the µRTM do not support SFP, the SFP-Tx signal from AMC should be terminated on the µRTM side.
If the AMC do not support SFP, the AMC should terminate SFP-CLK and SFP-Rx.
If the AMC do not support SFP, the AMC signal SFP-Tx should be open.

User Configuration:
The µRTM should let all unused signals open.
The AMC should let all unused signals open.

Digital fixed I/O:
If the µRTM do not support the signal function, the µRTM should terminate signals of this group.
If AMC_TCLK, OUT0 or OUT1 is not used (implemented) by the AMC, it should let them open.
If the µRTM support the signal function it has to provide a default logic state for the signals OUT0 and OUT1.

Digital Clock Inputs:
Unused digital clock inputs should be grounded on the µRTM side, signals are AC-coupled on the AMC side.
Unused digital clock inputs should be terminated on the AMC side.

Analog Inputs:
Unused analog AC-input or DC-input ports should be grounded on the µRTM.
Unused analog AC-input or DC-input ports should be shorted on the µRTM rear signal inputs to avoid oscillations at Zone 3.
Unused analog AC-input or DC-input ports can be open, terminated or grounded on the AMC side:

Open	: Recommended, especially if space and routing for a termination degrade the performance.
Terminated	: Can be used if space and routing for a termination do not degrade the performance.
(*) Grounded	: The AMC may only ground them if a functional or electrical compatibility check of Zone 3 is used. The robustness of boards against EMI is improved, but only compatible boards will be activated.

Analog Outputs:
Unused current driven DACs should be grounded on the µRTM.
Unused analog outputs should be grounded on the AMC.

Table 5 and Table 6 shows the signal termination if the AMC, respectively µRTM do not support a signal function. In case of not using the high speed link it should be switched off to avoid crosstalk onto the µRTM. Unused AC-input or DC-input ports should be open. Their rear signal inputs on the µRTM should be shorted to avoid oscillations at Zone 3. IF unused AC-input or DC-input ports are grounded to improve the EMI robustness only compatible boards will be activated via E-keying.

Class A1 / Zone			**a**	**b**	**c**	**d**	**e**	**f**
AMC side								
MTCA.4 management	J30	**1**	PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2	PWRA2	PWRB2	MP	SCL	TDI	TMS
FPGA / Standard Gbit-Link		**3**	open / differential terminated		open / differential terminated		open / open	open / open
FPGA User-configuration		**4**	open	open	open	open	open	open
		5	open	open	open	open	open	open
FPGA / Digital fixed I/O		**6**	open / open	open / open	open / open	open / open	open / open	open / open
Shielding		**7**	gnd	gnd	gnd	gnd	gnd	gnd
Digital clock inputs		**8**	differential terminated		differential terminated		differential terminated	
		9	differential terminated		differential terminated		differential terminated	
Shielding		**10**	gnd	gnd	gnd	gnd	gnd	gnd
Analog signals	J31	**1**	open / differential terminated / gnd *		gnd	gnd	open / differential terminated / gnd *	
		2	open / differential terminated / gnd *		gnd	gnd	open / differential terminated / gnd *	
		3	open / differential terminated / gnd *		gnd	gnd	open / differential terminated / gnd *	
		4	open / differential terminated / gnd *		gnd	gnd	open / differential terminated / gnd *	
		5	open / differential terminated / gnd *		gnd	gnd	open / differential terminated / gnd *	
		6	open / differential terminated / gnd *		gnd	gnd	open / differential terminated / gnd *	
		7	open / differential terminated / gnd *		gnd	gnd	open / differential terminated / gnd *	
		8	open / differential terminated / gnd *		gnd	gnd	open / differential terminated / gnd *	
		9	open / differential terminated / gnd *		gnd	gnd	open / differential terminated / gnd *	
		10	open / differential terminated / gnd *		gnd	gnd	open / differential terminated / gnd *	

Table 5: Signal termination in Class A1 if the AMC do support a signal function, AMC side view

Class A1 / Zone			**a**	**b**	**c**	**d**	**e**	**f**
RTM side								
MTCA.4 management	J30	**1**	PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2	PWRA2	PWRB2	MP	SCL	TDI	TMS
FPGA / Standard Gbit-Link		**3**	open / open	open / open	open / open	open / open	open / differential terminated	
FPGA User-configuration		**4**	open	open	open	open	open	open
		5	open	open	open	open	open	open
FPGA / Digital fixed I/O		**6**	open / differential terminated		open / differential terminated		open / differential terminated	
Shielding		**7**	gnd	gnd	gnd	gnd	gnd	gnd
Digital clock inputs		**8**	gnd	gnd	gnd	gnd	gnd	gnd
		9	gnd	gnd	gnd	gnd	gnd	gnd
Shielding		**10**	gnd	gnd	gnd	gnd	gnd	gnd
Analog signals	J31	**1**	gnd	gnd	gnd	gnd	gnd	gnd
		2	gnd	gnd	gnd	gnd	gnd	gnd
		3	gnd	gnd	gnd	gnd	gnd	gnd
		4	gnd	gnd	gnd	gnd	gnd	gnd
		5	gnd	gnd	gnd	gnd	gnd	gnd
		6	gnd	gnd	gnd	gnd	gnd	gnd
		7	gnd	gnd	gnd	gnd	gnd	gnd
		8	gnd	gnd	gnd	gnd	gnd	gnd
		9	gnd	gnd	gnd	gnd	gnd	gnd
		10	gnd	gnd	gnd	gnd	gnd	gnd

Table 6: Signal termination in Class A1 if the µRTM do support a signal function, µRTM side view

SUBCLASSES AND CLASS COMPATIBILITY

During the introduction of the class concept and operation of boards it turned out, that the needs for the user zone (J30 row 3-6) of applications differs by a slightly different signals in the user-configuration zone. Using classes as identifiers for a simple board activation, especially for existing boards, subclasses have to be introduced to guarantee the electric safe board activation. Table 7 summarizes the actual subclasses (status 08/2014, Rev.4) called A1.0, A1.0C, A1.1CO. The appendix describes the subclass, in detail the number of high speed links, “C” for the AMC_TCLK clock option and “O” for the output option OUT0, OUT1 support.

Subclass A1.0			**a**	**b**	**c**	**d**	**e**	**f**
Pin-assignment								
FPGA	J30	**3**	D0+	D0-	D1+	D1	D2+	D2-
FPGA User-configuration		**4**	D3+	D3-	D4+	D4-	D5+	D5-
		5	D6+	D6-	D7+	D7-	D8+	D8-
FPGA		**6**	D9+	D9-	D10+	D10-	D11+	D11-
Electrical specification								
FPGA	J30	**3**	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O
FPGA User-configuration		**4**	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O
		5	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O
FPGA		**6**	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O
Quiescent condition								
FPGA	J30	**3**	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
FPGA User-configuration		**4**	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		5	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
FPGA		**6**	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA

Subclass A1.0C			**a**	**b**	**c**	**d**	**e**	**f**
Pin-assignment								
FPGA	J30	**3**	D0+	D0-	D1+	D1	D2+	D2-
FPGA User-configuration		**4**	D3+	D3-	D4+	D4-	D5+	D5-
		5	D6+	D6-	D7+	D7-	D8+	D8-
FPGA / Digital fixed I/O		**6**	AMC_TCLK+	AMC_TCLK-	D10+	D10-	D11+	D11-
Electrical specification								
FPGA	J30	**3**	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O
FPGA User-configuration		**4**	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O
		5	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O
FPGA / Digital fixed I/O		**6**	LVDS - O	LVDS - O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O
Quiescent condition								
FPGA	J30	**3**	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
FPGA User-configuration		**4**	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		5	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
FPGA / Digital fixed I/O		**6**	Disabling via Buffer	Disabling via Buffer	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA

Subclass A1.1CO			**a**	**b**	**c**	**d**	**e**	**f**
Pin-assignment								
Standard Gbit-Link	J30	**3**	SFP-CLK+	SFP-CLK-	SFP-RX+	SFP-RX-	SFP-TX+	SFP-TX-
FPGA User-configuration		**4**	D3+	D3-	D4+	D4-	D5+	D5-
		5	D6+	D6-	D7+	D7-	D8+	D8-
Digital fixed I/O		**6**	AMC_TCLK+	AMC_TCLK-	OUT0+	OUT0-	OUT1+	OUT1-
Electrical specification								
Standard Gbit-Link	J30	**3**	LVDS-I	LVDS-I	CML-I	CML-I	CML-O	CML-O
FPGA User-configuration		**4**	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O
		5	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O
Digital fixed I/O		**6**	LDVS-O	LDVS-O	LDVS-O	LDVS-O	LDVS-O	LDVS-O
Quiescent condition								
Standard Gbit-Link	J30	**3**			Idle state, RTM AC-coupled	Idle state, RTM AC-coupled	Idle state, AMC AC-coupled	Idle state, AMC AC-coupled
FPGA User-configuration		**4**	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
		5	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
Digital fixed I/O		**6**	Disabling via Buffer	Disabling via Buffer	Disabling via Buffer	Disabling via Buffer	Disabling via Buffer	Disabling via Buffer

Table 7: Subclass definition Class A1.0, A1.0C, A1.1CO (“I”=input (µRTM to AMC), “O”=output (AMC to µRTM)), AMC side view

Class compatibility can be easily achieved by using assembly options, mainly on the AMC board. The appropriate assembly setting must be listed in the AMC and RTM FRU for board activation. µRTM boards typically have a record of electrical compatible classes of AMC boards. Due to the fact, that high speed links and the OUT0 and OUT1 signals typically represents system relevant signals – not dependent of FPGA firmware issues, we recommend not to use electronic switches. To avoid reflections and to achieve a class compatibility we recommend, as depicted in Table 5,6 the termination of unused signals of row 6 on the µRTM. Appropriate schematic templates and evaluation boards are available on http://mtca.desy.de.

REVISION CHANGES AND HISTORY

2010/05 : - Separated AC-coupled and DC-coupled inputs at Zone 3.
Separation:
(+) Zone 3 voltage ranges and levels are defined independent of specific ADC signal-conditioning and leveling.
(-) Space needed and assembly variants exists on the AMC side.
No separation :
(+) ADC signal conditioning is only defined on the µRTM.
(+) No top-layer jumper selection is needed -> High speed applications.
( ) ADC front-end has to be terminated by a network on the ACM side.
(-) OP-Amp input stages share a VCM line with ADC -> needs VCM signal over Zone 3, e.g. J31, 2,4,6,8,10
(-) ADC input stage widely distributed over Zone 3 -> EMI distortions have to be tested.

2012/01 (Rev.A.1) : - DAC channels were extended in (J31 column cd) to be compatible with the AMC520 Vadatech product.
2012/01 (Rev.A.1) : - DAC RTM_CLK4 was placed for using a different DAC and ADC sampling rate.
2012/03 (Rev.A.1) : - FPGA RTM_CLK5 was placed to synchronize µRTM circuits with the AMC module.
2012/03 (Rev.A.1) : - RTM_CLK2, RTM_CLK3 was placed for multi-channel direct sampling AMC modules.
2012/06 (Rev.A.1) : - GTP was placed in (J30 row 3) for future upcoming µRTM boards.
2012/06 (Rev.A.1) : - I^2C for general µRTM diagnostics is placed.
2012/06 (Rev.A.1) : - ps-stable RESET signal was placed to reset divider phases after power cuts reproducible.
2012/06 (Rev.A.1) : - INTERLOCK1, INTERLOCK2 were introduced to drive µRTMs with vector modulators for high power applications.
2012/06 (Rev.A.1) : - Power Off quiesce action process using a hot-swap handle µRTM is proposed for transient current protection.

2012/11 (Rev.A.2) : - Timing clock AMC_TCLK (splitted from TCLKA) moved to (J30 6ab) and replaces RESET
-> A RESET circuit is µRTM specific and should be used on the µRTM
-> AMC_CLK signal and a course RESET from Dx (J30 row 4,5) provides a local ps-stable RESET option.
-> TCLKA length compensation should be done in the MCH, where they are splitted.
2012/11 (Rev.A.2) : - I^2C bus (4 ab) removed and will be emulated by the FPGA on Dx (J30 row 4,5).
2012/11 (Rev.A.2) : - INTERLOCKx signals renamed to general purpose outgoing signals OUT0, OUT1 (J30 6cd, J30 6ef)
2012/11 (Rev.A.2) : - VADATECH, STRUCK and SLAC agreed to DAC filling sequence starting from (DAC0+, DAC0-)
(+) To reduce signal crosstalk AC, DC channels starts from channel 0 contrary to the DAC filling order.
2012/11 (Rev.A.2) : - Isolation of AMC_TCK, OUT0, OUT1, DACx is realized for the quiesce action and replaces AMC power off.
-> MMC controls disabling AMC_TCLK, OUT0, OUT1 via buffers on the AMC side.
-> MMC inform FPGA to disable SFP, Dx signals and DAC quiescent condition.

2012/12 (Rev.A.3) : - LVDS for low-jitter clocks (J30 row 8,9) are performance limited.
-> Improve compatibility to LVDS, LVPECL, CML and other clocks by using differential AC-coupling.
2013/01 (Rev.A.3) : - Preparation for future FPGA bank voltages for LVCMOS and OC signals
-> Concerns only LVCMOS and OC signals pull-up voltages, LVDS transport s only currents.
-> Introduce an µRTM voltage adjustment mechanism provided by the management via I^2C DAC on the RTM side.
(Similar mechanism to FMC Vita57.1, but without using extra pins on Zone 3)
2013/02 (Rev.A.3) : - DACx outputs should be able to be shorted to GND on the µRTM side.
-> Improve GND-GND Zone 3 connection and channel isolation.
-> DACx outputs should be current driven, so far no conflicts with existing boards on the market.
-> Zone 3 grounding, shielding and termination defined for reduced functionalities.

2013/03 (Rev.A.3) : - BoF group1 Zone 3 pin assignment (Class recommendation) Rev.A.3. in confirmation status.
-> Software E-keying section removed -> Part of BoF group IPMI or MMC.

2014/08 (Rev.A.4) : - Introduction of subclasses in the user zone.
-> Using class identifiers for a simple board activation requires to have identifiers for all boards.
-> Different applications require a slightly different user-zone pin-assignment, especially for a limited number of pins.
-> Class compatibility can be easily achieved by using assembly options.
2014/08 (Rev.A.4) - Idle state, AC-coupling for SFP signals must be done on the transmitter side, AC-coupling on the receiver side can be done.
- Low jitter clocks AC-coupling has to be done before termination on the AMC-side.
2014/08 (Rev.A.4) -> To avoid stub elements and improve the signal quality modern low-jitter chips uses internal termination after AC-coupling.
2014/08 (Rev.A.4) : - Class recommendation Rev.A.4. has to go into the confirmation status.
-> BoF group 1, PICMG