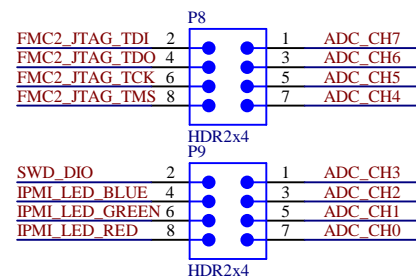
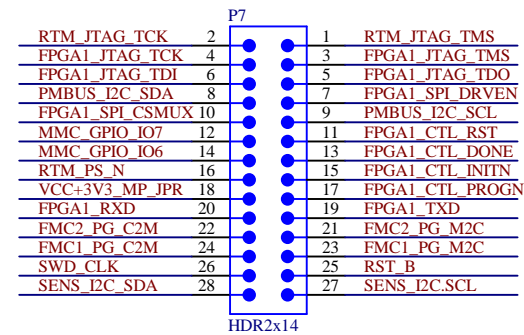
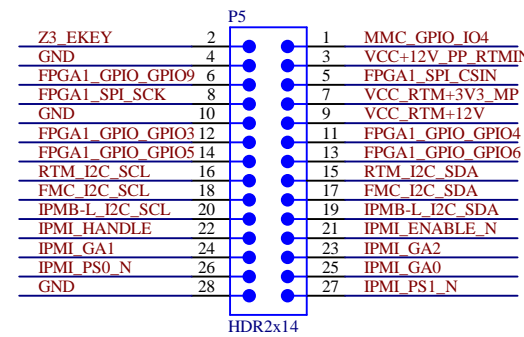
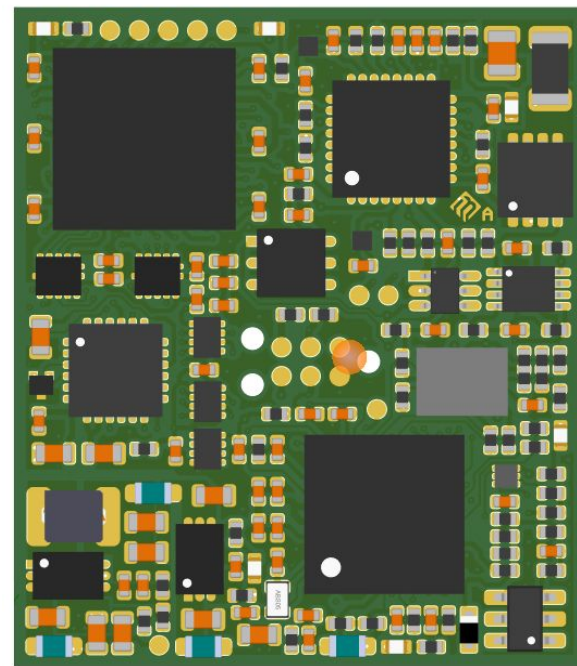
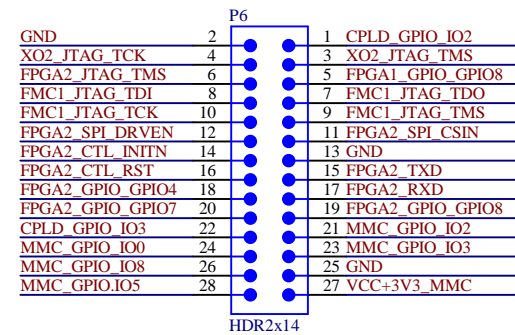
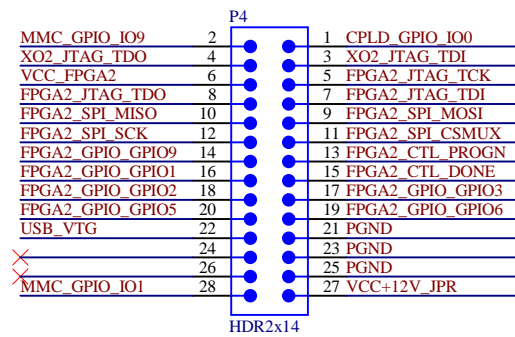
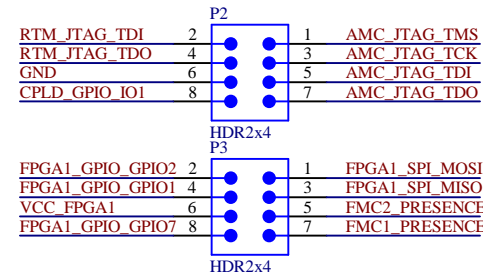


DMMC-STAMP Breakout Board LC

Pin Headers

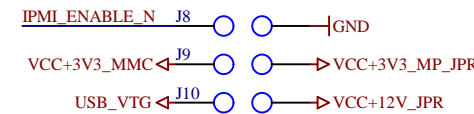


Tag Connect TC2030 Plug (on LGA Module)

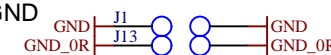


Debug Jumpers (Standalone Operation)

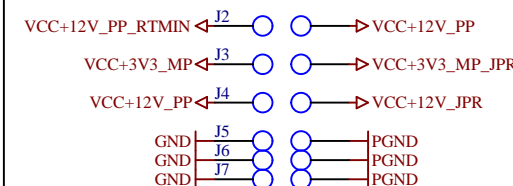
Caution: Voltages can be shorted here. Read the manual!



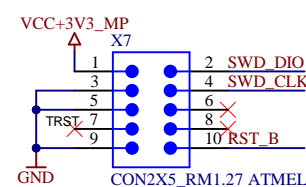
Extra GND



Current Measurement Jumpers

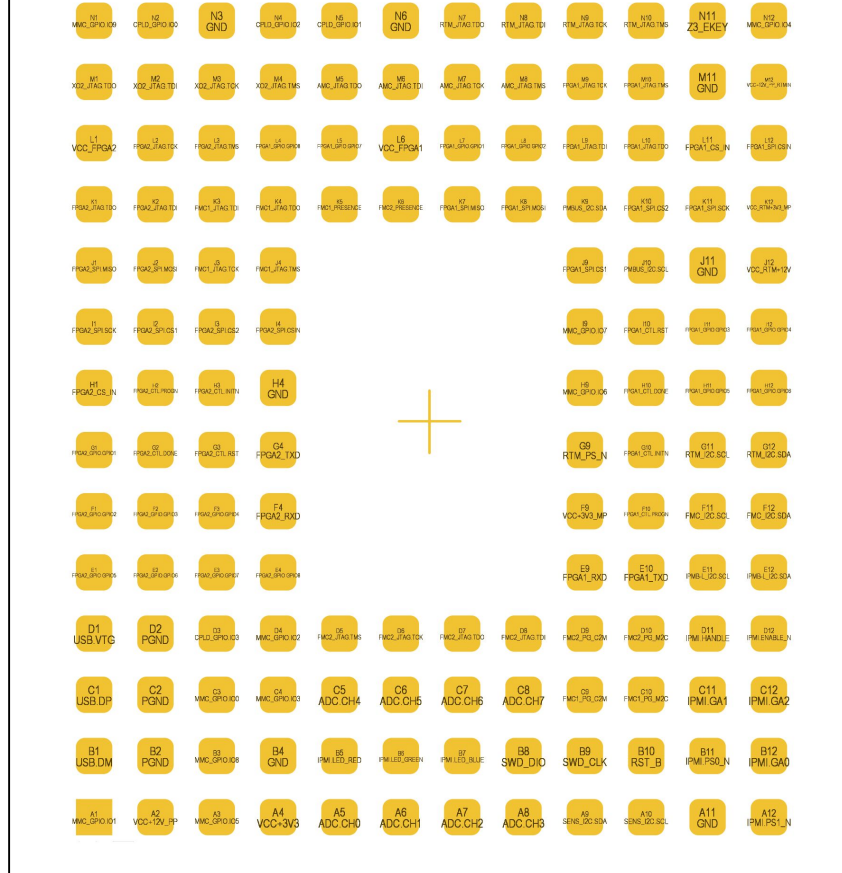


MCU JTAG Port (optional, MMC-STAMP has on-board JTAG "plug of nails" socket)

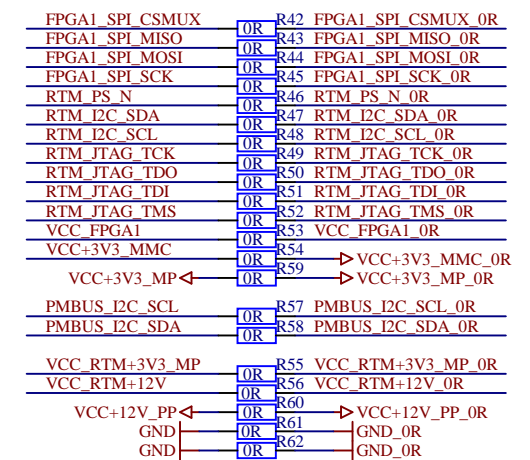


Name	AVR port pin	SAM port pin	Description
SWDCLK	1	4	Serial Wire Debug Clock.
SWDIO	5	2	Serial Wire Debug Data Input/Output.
SWO	3	6	Serial Wire Output (optional- not implemented on all devices).
nRST	6	10	Reset.
VTG	4	1	Target voltage reference.
GND	2, 10	3, 5	Ground.

LGA Footprint (Top View)



OR Bridges for to optional MTCA.4 Module



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Project Title:
DMMC-STAMP-BreakOutLC.PrjPCB
Schematic Title:
LGA Footprint (2mm pitch)
DATE: 15.12.2019 21:04:28



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Engineer 1: Michael Feniner
Engineer 2: S. Chystiakov / J.Zink

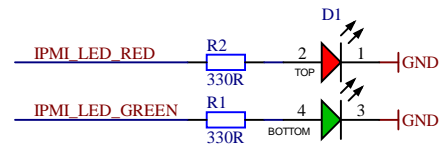
Rev: B
Size: A3
Sheet:

FILENAME: Debug.SchDoc

1 of 3

Mandatory Components on AMC Card

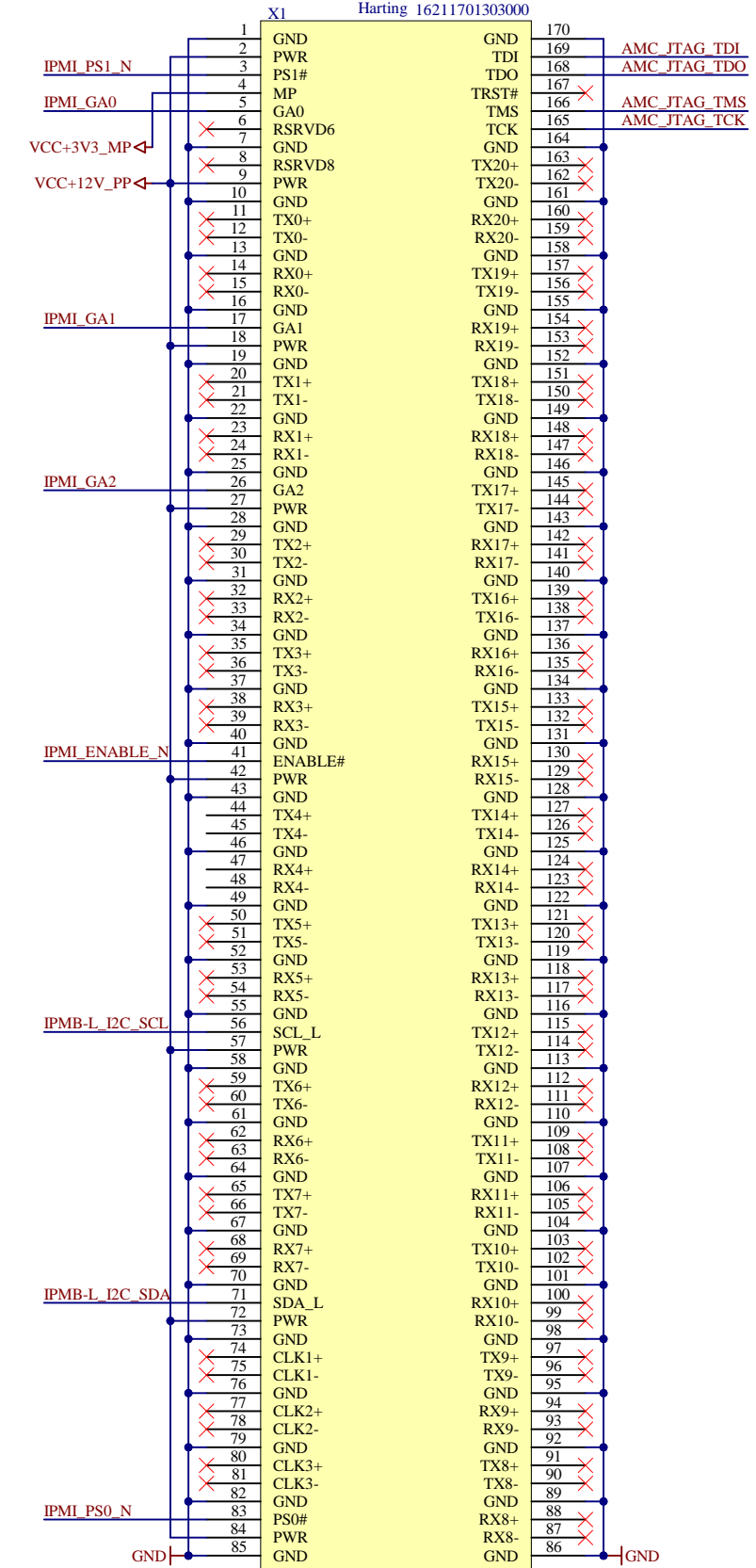
IPMI LEDs (fault / OK)



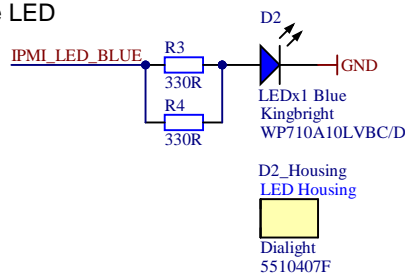
MMC Stamp LGA Module



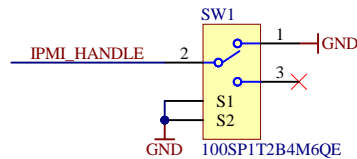
AMC Connector



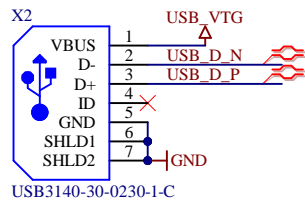
Blue LED



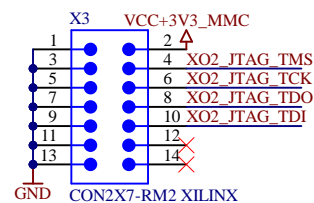
MicroTCA Handle Dummy



USB Debug Connector (recommended)



Xilinx JTAG IN (recommended)



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Project Title:
DMMC-STAMP-BreakOut.LC.PrjPCB
Schematic Title:
Mandatory Components
DATE: 14.08.2020 21:04:28



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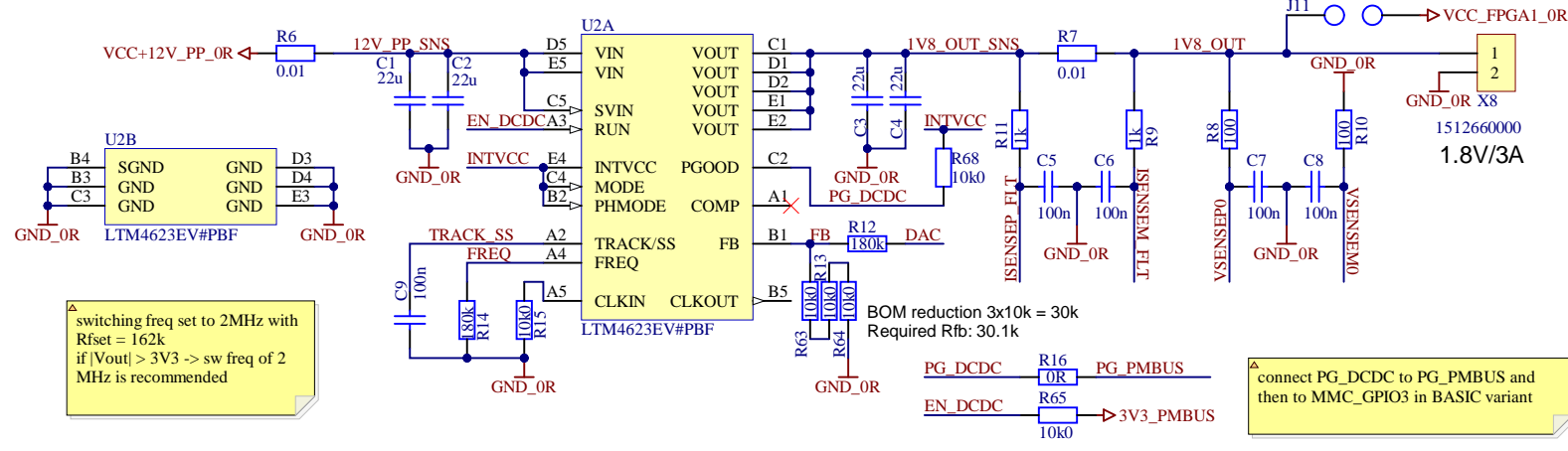
Engineer 1: Michael Feniner
Engineer 2: S. Chystiakov / J.Zink

Rev: B
Size: A3
Sheet:
2 of 3

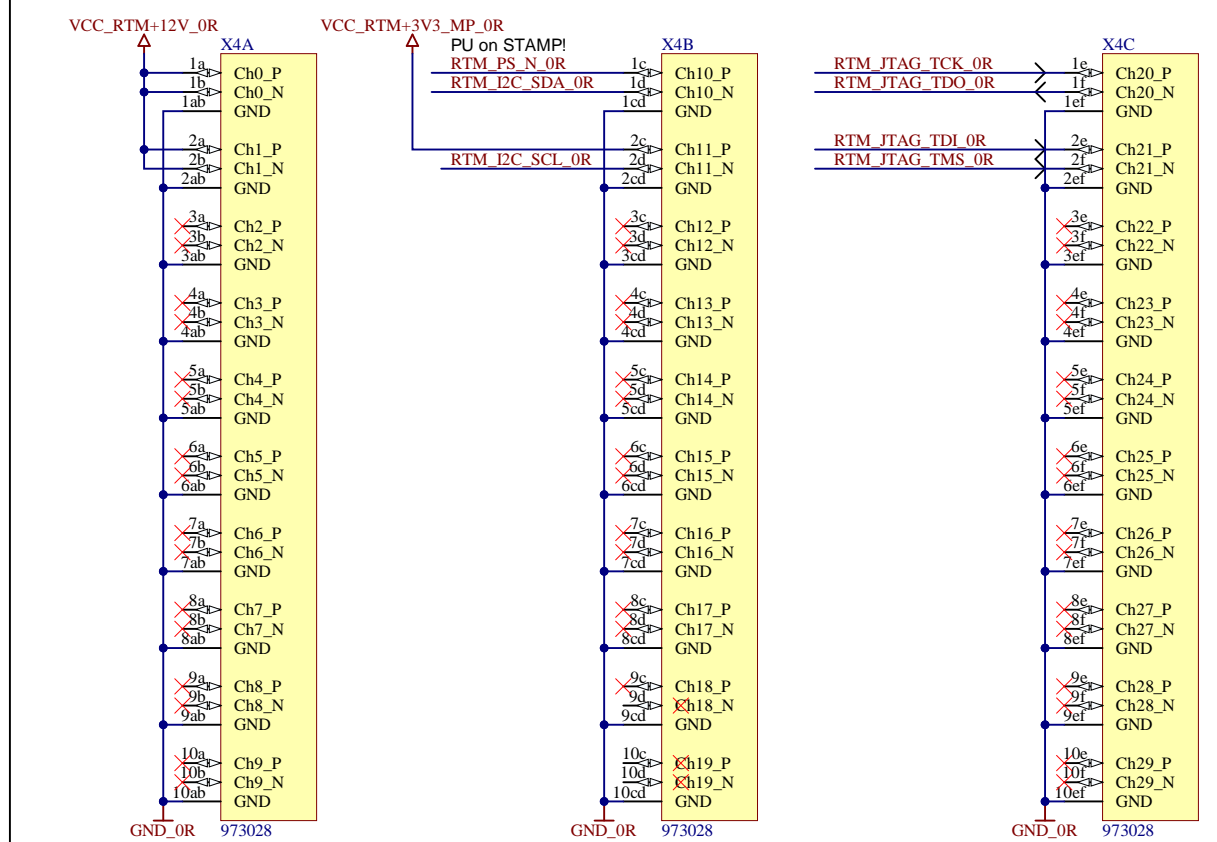
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Example Peripherals: Power, PMBUS(TM), Flash, FPGA JTAG, Zone3

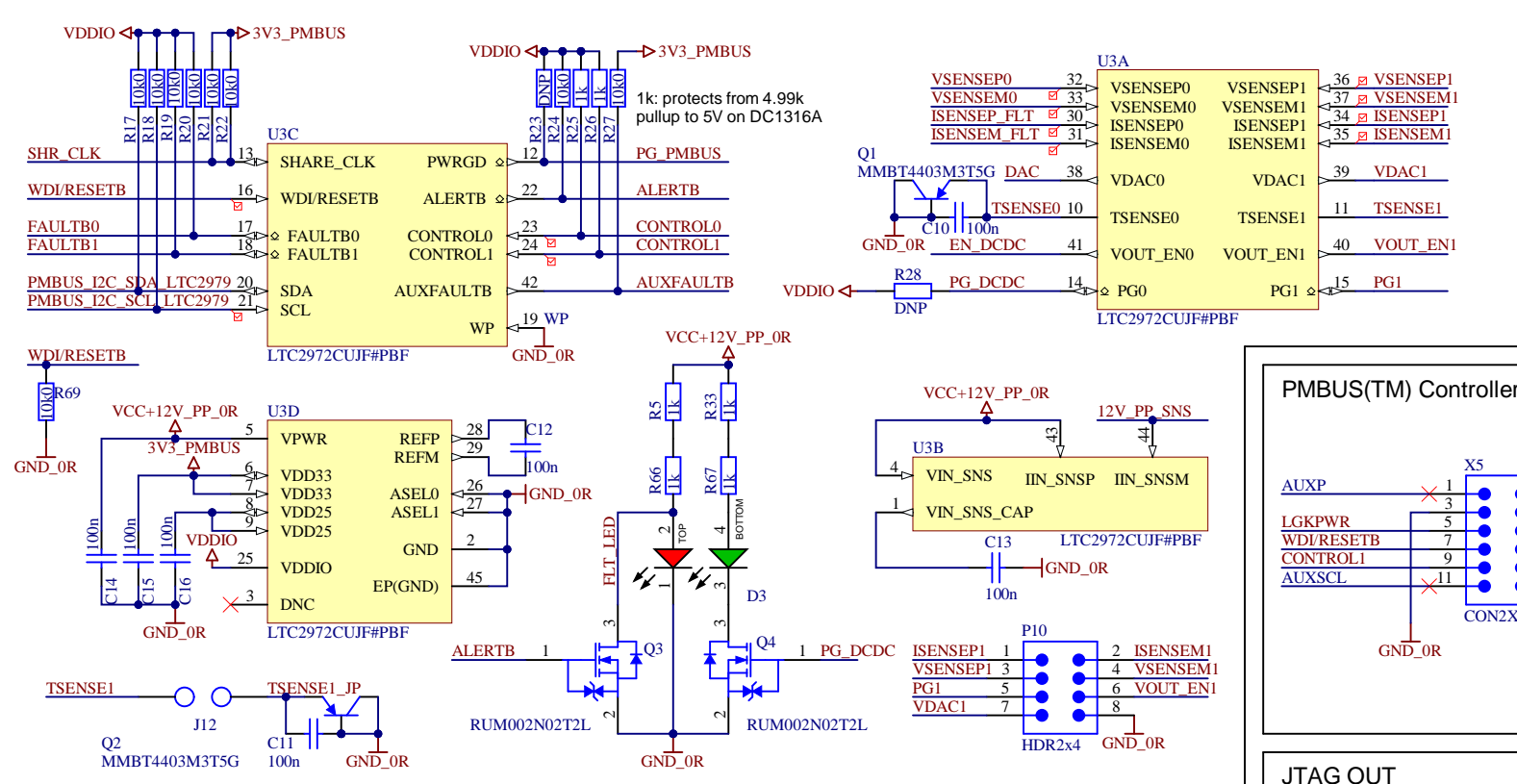
Example Low EMI 3A uModule(TM) DCDC Converter



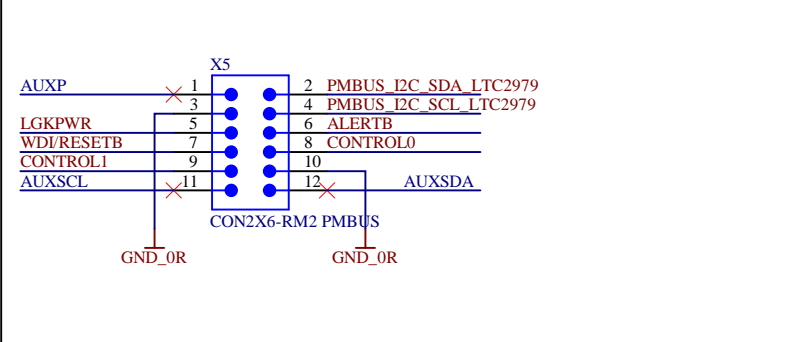
Zone 3 Power, Management, JTAG (optional)



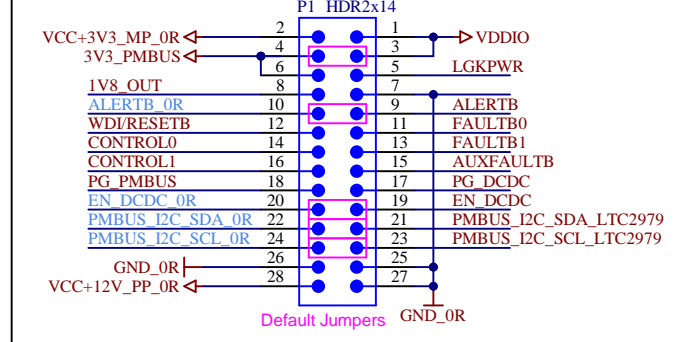
Example Two-Channel PMBUS(TM) Controller with Accurate Voltage/Current/Temperature Sensing



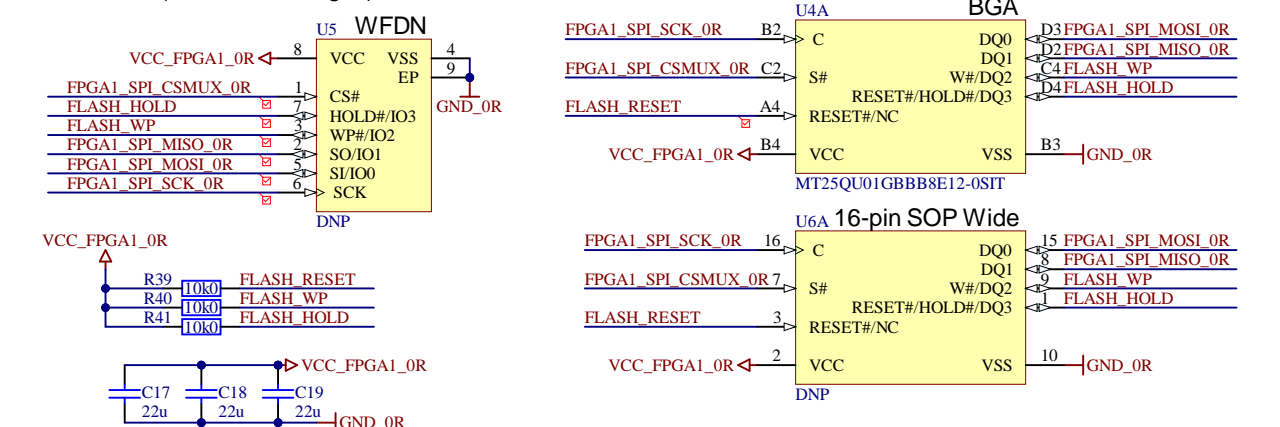
PMBUS(TM) Controller PC Interface (DC1613A)



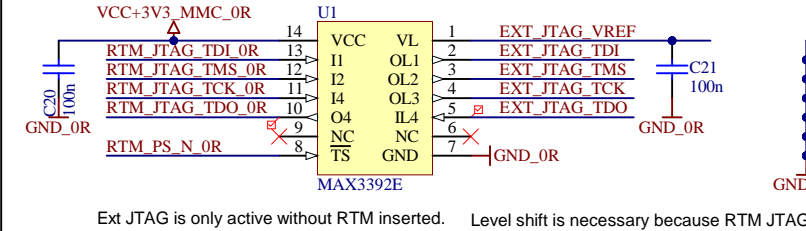
PMBUS(TM) Debug



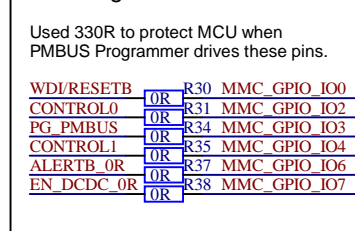
FPGA1 Flash (different Packages)



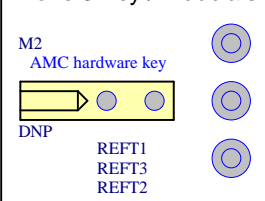
JTAG OUT



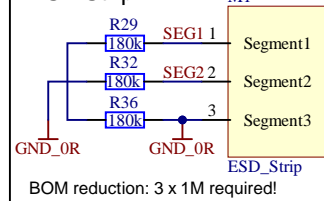
OR Bridges



Zone 3 Key / Fiducials



ESD Strip



Project Title:
DMMC-STAMP-BreakOut.LC.PrjPCB

Schematic Title:
Optional Components

DATE: 10.12.2020 21:04:28

Engineer 1: Michael Feniner
Engineer 2: S. Chystiakov / J.Zink

Rev: B
Size: A3
Sheet: 3 of 3

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FILENAME: Optional.SchDoc