DAMC-FMC1Z7IO

VERSION 2.0

Highlights

- **Cost-optimized FMC carrier and IO controller board**
- **Xilinx® Zynq®-7000 SoC: XC7Z030 (default), XC7Z035 and XC7Z045**
- **Full Backplane and RTM connectivity**
- **48 bidirectional IOs: 3.3V and true 5V**
- **Front Micro-HDMI and USB Ports**
- **Board Support Package including Yocto Embedded Linux available**

Features

Based on Xilinx® Zynq®-7000 System-on-Chip hosting Dual-Core ARM® Cortex-A9 Processor
FMC LPC socket with up to 4 transceivers
Zone3 RTM interface according to DESY class D1.0
PCIe x2 Gen.2 supported, x4 as configuration option
1GB DDR3 memory connected to the PS
Front panel SMA connector for external clock input
Flexible clocking system
MicroSD card slot to host operating system
Redundant flash and eMMC memory to host operating system
Preprogrammed CPLD for more flexibility on front panel and backplane IO
Complete AMC power management via PMBUS™

The DAMC-FMC1Z7IO is a cost optimized Xilinx® Zynq®-7000 based IO controller and signal processing board with one FMC socket in MicroTCA.4 AMC form factor. It can be equipped with Xilinx XC7Z030, XC7Z035 or XC7Z045 SoCs. The programmable logic features 125k/275k/350k logic cells, 400/900/900 DSP slices and 4x/8x/8x Multi-Gigabit Transceivers running at up to 12.5Gbps.

All MTCA.4 backplane ports are connected to the SoC. Gigabit Ethernet (backplane port 0) is connected to the Processing System (ARM®) which provides a flexible platform e.g. for running application servers. Eight M-LVDS timing/trigger signals and three TCLK backplane clock lines are connected as well. The board features a DDR3 memory block with 1GB (32bits) connected to PS, operating at 1066 MHz.

The DAMC-FMC1Z7IO has one FMC LPC socket that has 2/4 transceivers connected (HPC connector) to the SoC. To ensure a safe connection of FMC or RTM cards an appropriate compatibility check is performed by the management firmware running on the DMMC-STAMP

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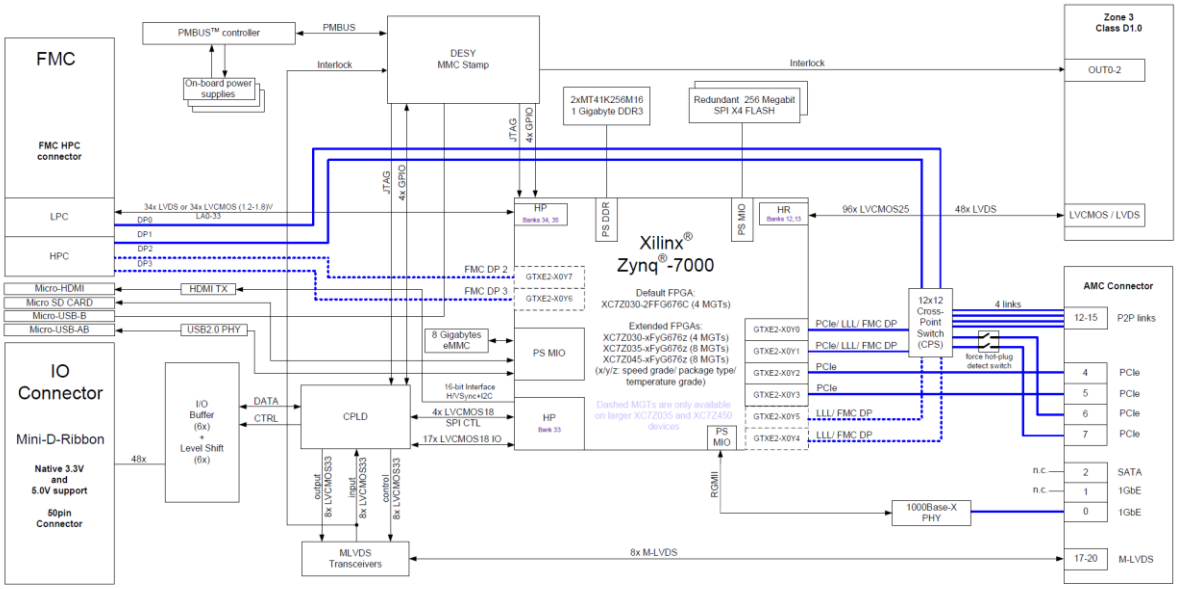

Figure 1: DAMC-FMC1Z7IO block diagram

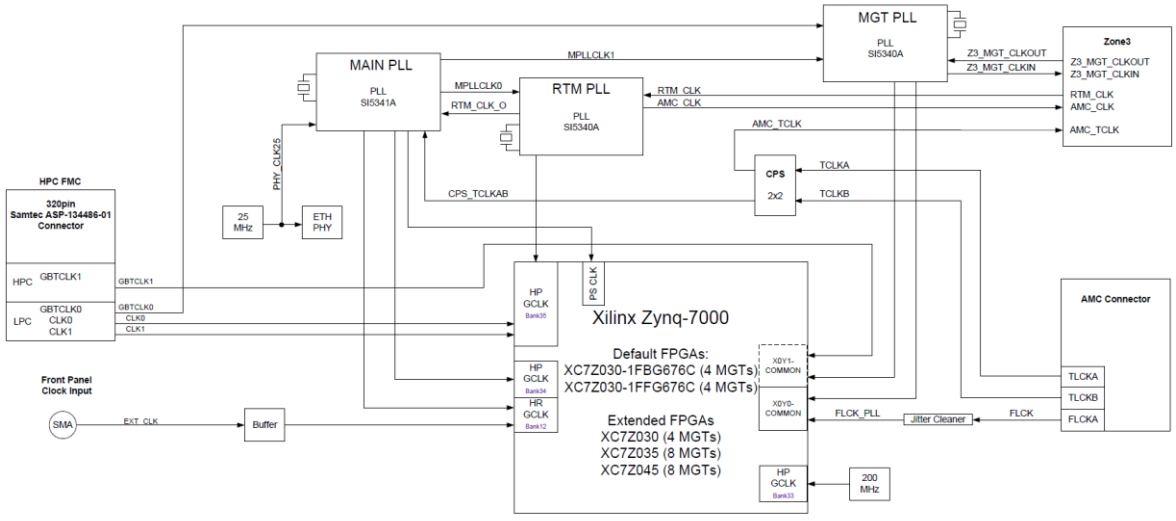

Figure 2: DAMC-FMC1Z7IO clock scheme